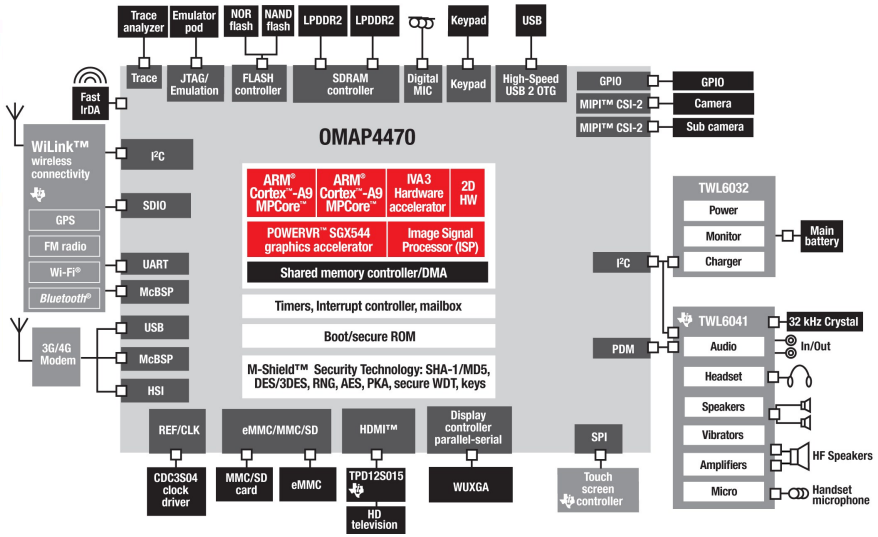
The striVe RISC-V Open SoC Family using SkyWater 130nm Process

Apache 2.0-Licensed

from Software to Silicon

I designed chips for stuff



Kindle Fire HD

Kindle Fire

Droid Razr

Droid X

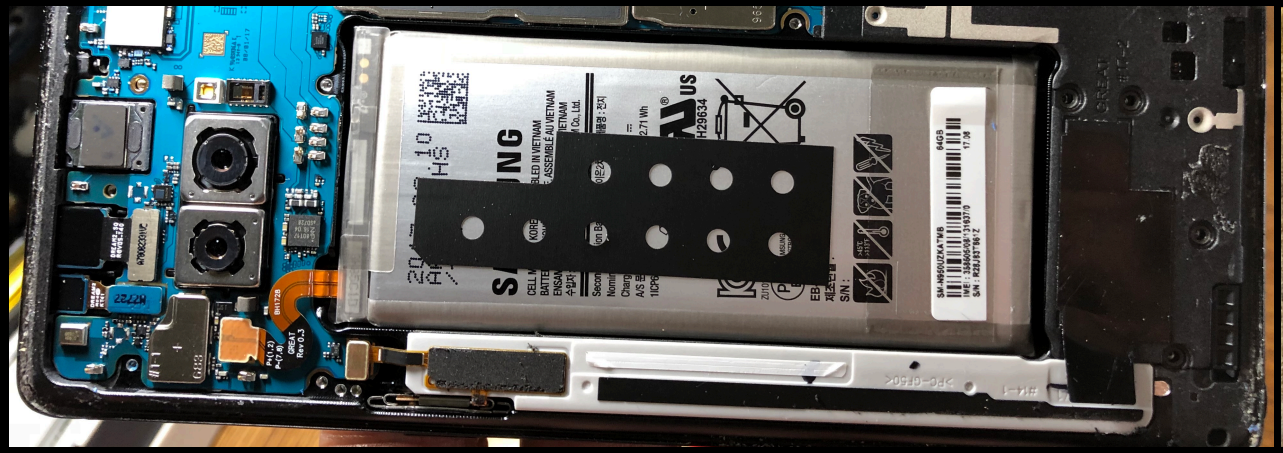
Huawei Ascend D1

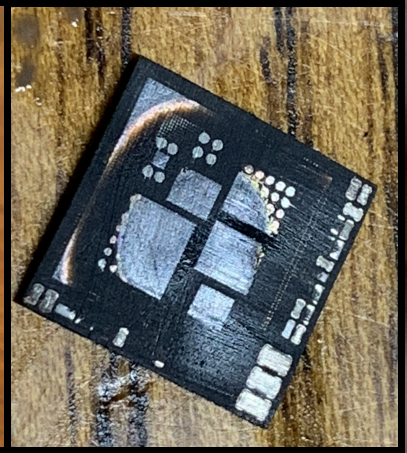
Motorola - Droid Milestone

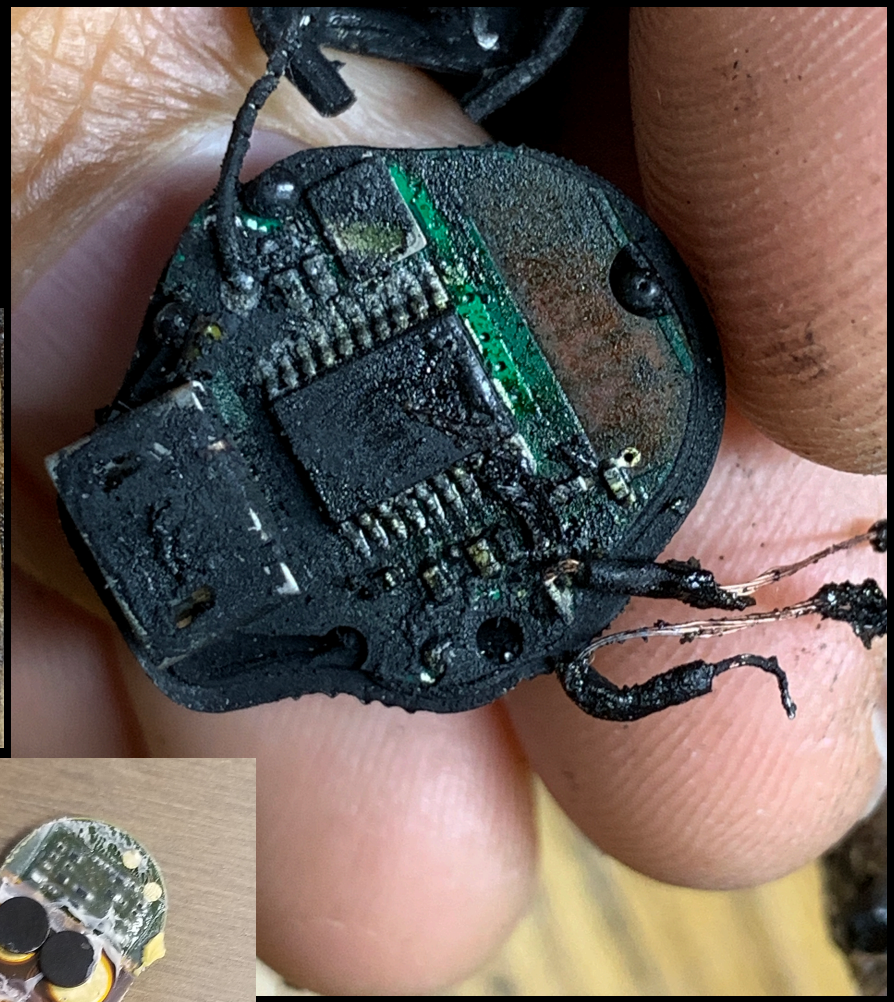
Motorola - Droid Bionic

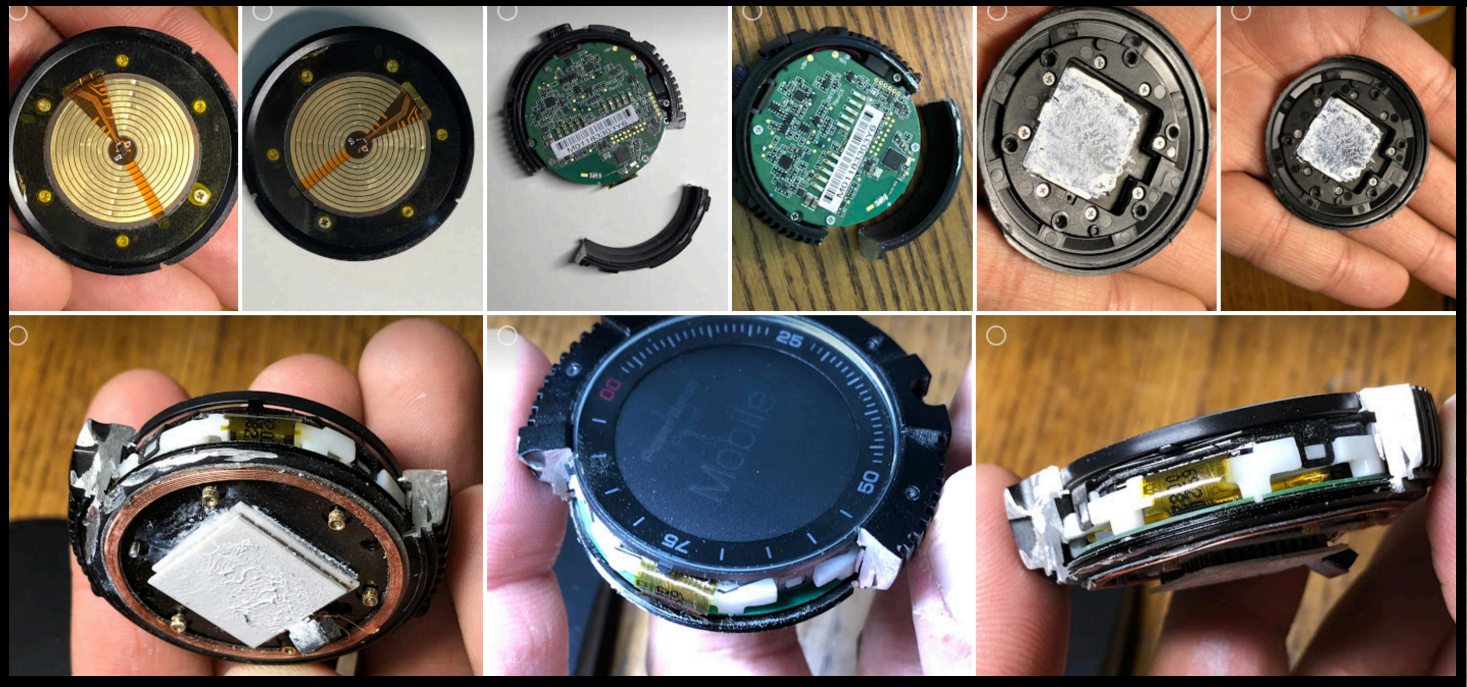
Mohamed

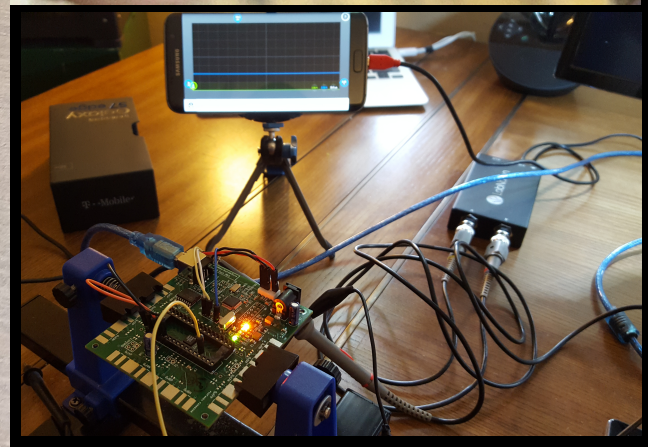
I break other stuff











efabless.com

Co-founder & CTO

We make it possible for anyone

To design Open Source ASICs

RECAP of July/August 2020

THE PDK RELEASE

June 30, 2020

Google + skywater TECHNOLOGY

FOSS 130nm Production PDK

github.com/google/skywater-pdk

License - Apache 2.0

THE APACHE™ SOFTWARE FOUNDATION

open source initiative®

Approved License

j.mp/du20-sky130

Hosted on GitHub#

skywater TECHNOLOGY FOUNDRY Google

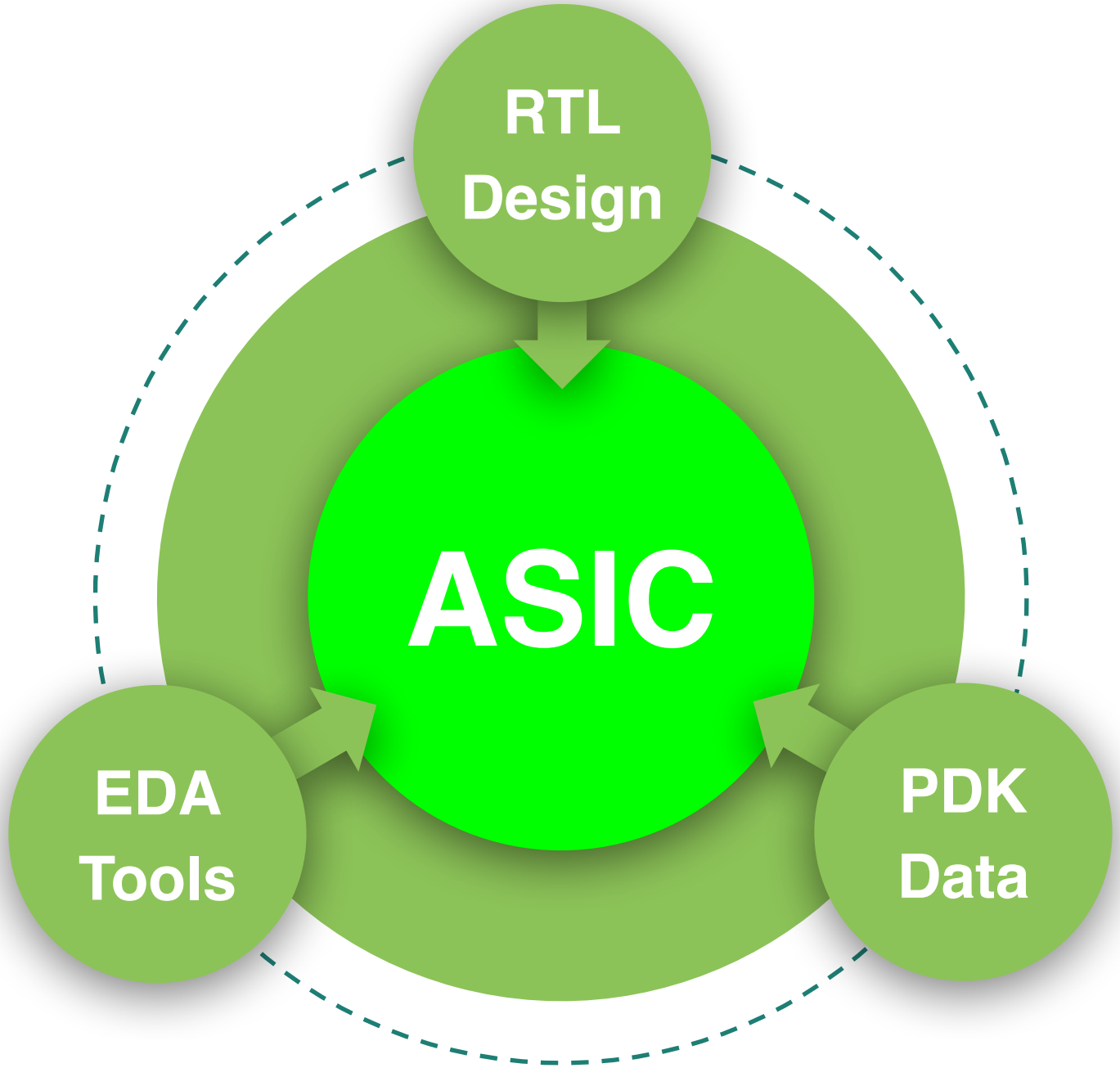
github.com/google/skywater-pdk

No NDA, nothing to sign^, just clone and run: *make timing*

google / skywater-pdk Unwatch 115 Unstar 1.2k Fork 114

Some larger bits in submodule on foss-eda-tools.googlesource.com
^ Google CLA require to contribute to repository

j.mp/du20-sky130



Fully open ASIC!

Google + skywater TECHNOLOGY

FOSS 130nm Production PDK
github.com/google/skywater-pdk

j.mp/du20-sky130

"Just" Digital Standard Cells

Library Name	Type	Cells
sky130_fd_sc_hd sky130_fd_sc_hdll	High Density + Low Leakage	**163** **111**
sky130_fd_sc_hvl	High Voltage	**56**
sky130_fd_sc_hs sky130_fd_sc_ms sky130_fd_sc_ls	High Speed Medium Speed Low Speed	**150** **150** **153**
sky130_fd_sc_lp	Low Power	**186**

j.mp/du20-sky130

The current status

1. [Done] Digital Standard Cells
2. [Done] Base primitives + Automated DRC
3. [TODO] Analog /RF primitives/
4. [TODO] IO and Periphery Cells
5. [TODO] Build spaces for SRAM^ / Flash
6. [TODO] OpenRAM SRAM Compiler

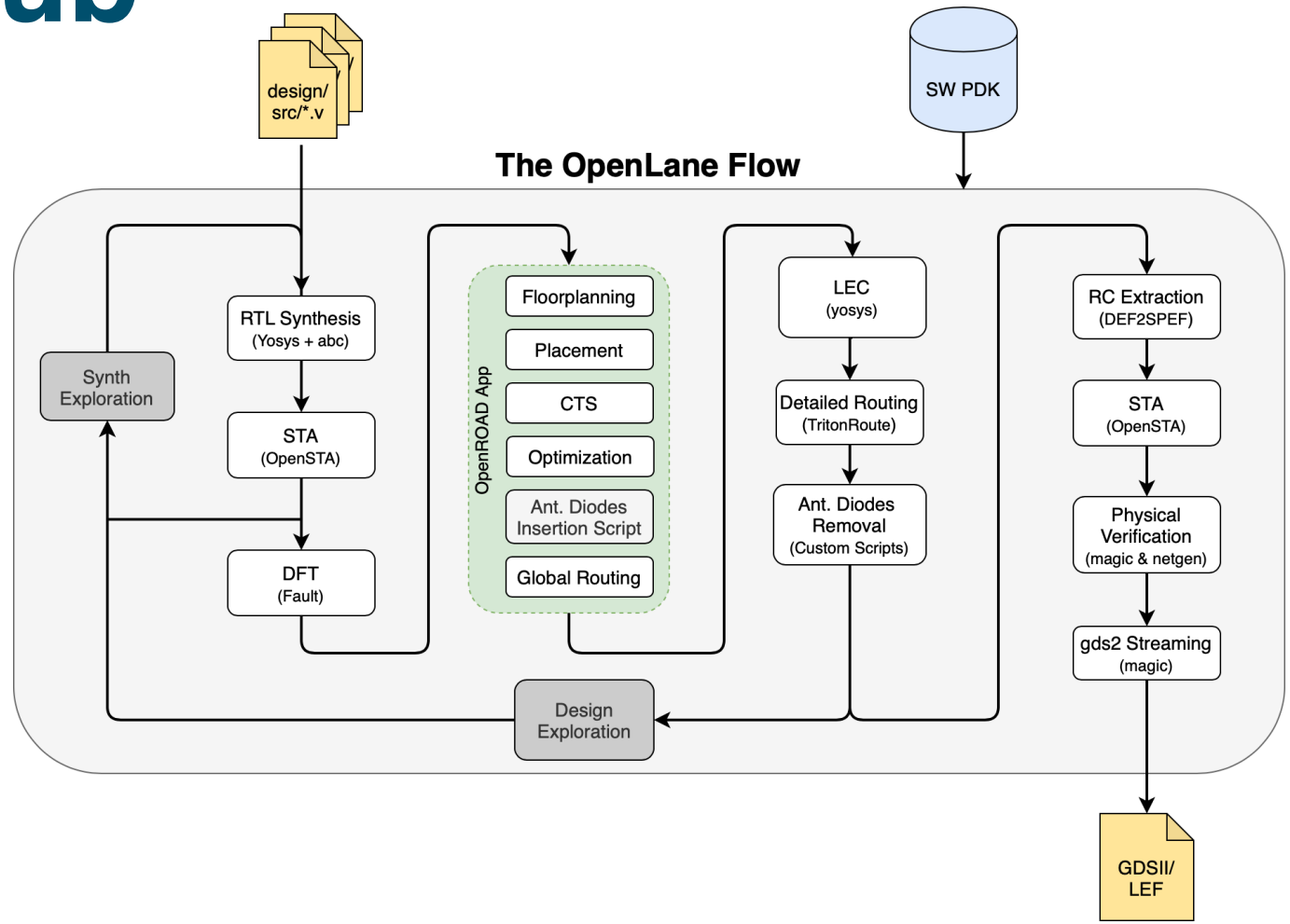
j.mp/du20-sky130

THE DEISGN FLOW

RELEASE

Hosted on GitHub#

- Digital IP - released
- SoC support in days
- Includes examples
- Complete GDSII



efabless / openlane

Watch 17 | Unstar 111 | Fork 22

openlane.io

Now what ....

What can I do with the 130nm process?

Intel Chips

13

2000
Intel® Pentium® 4 processor

Initial clock speed:
1.5GHz

Transistors:
42 million

Manufacturing technology:
0.18 micron

14

2001
Intel® Xeon® processor

Initial clock speed:
1.7GHz

Transistors:
42 million

Manufacturing technology:
0.18 micron

15

2003
Intel® Pentium® M processor

Initial clock speed:
1.7GHz

Transistors:
55 million

Manufacturing technology:
90nm

16

2006
Intel® Core™2 Duo processor

Initial clock speed::
2.66GHz

Transistors:
291 million

Manufacturing technology:
65nm

17

2008
Intel® Core™2 Duo processor

Initial clock speed:
2.4GHz

Transistors:
410 million

Manufacturing technology:
45nm

18

2008
Intel® Atom™ processor

Initial clock speed:
1.86GHz

Transistors:
47 million

Manufacturing technology:
45nm

19

2010
2nd generation Intel® Core™ processor

Initial clock speed:
3.8GHz

Transistors:
1.16 billion

Manufacturing technology:
32nm

20

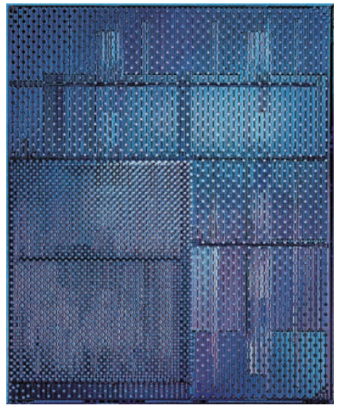
2012
3rd generation Intel® Core™ processor

Initial clock speed:
2.9GHz

Transistors:
1.4 billion

Manufacturing technology:
22nm


13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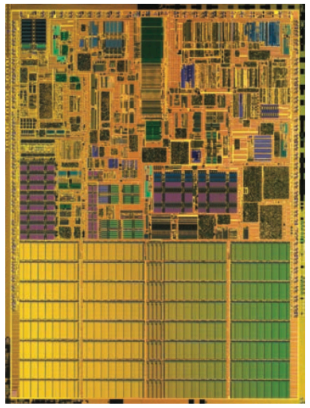
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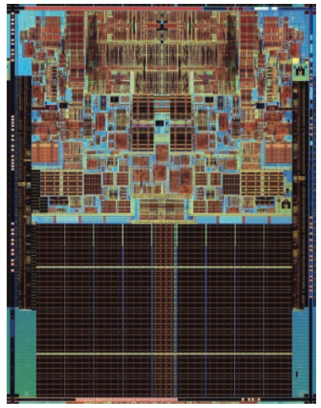
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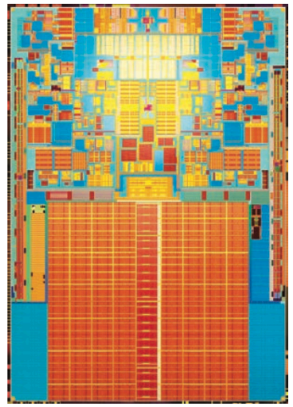
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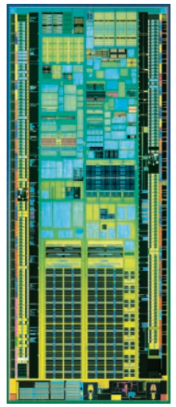
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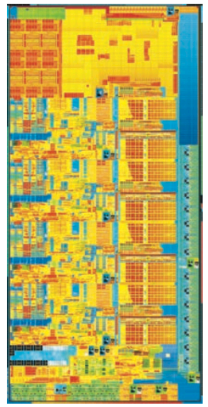
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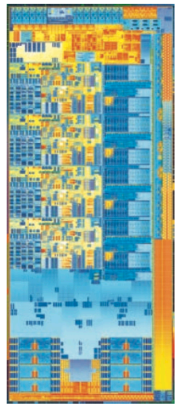
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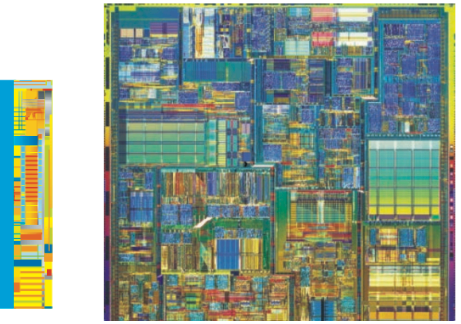
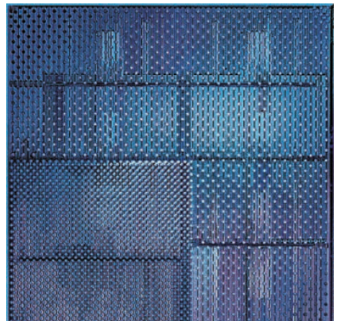
Intel Chips





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47 million

Manufacturing technology:
45nm

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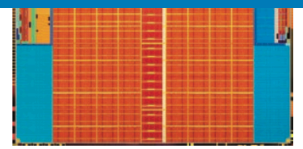
Manufacturing technology:
32nm

1.4 billion

Manufacturing technology:
22nm



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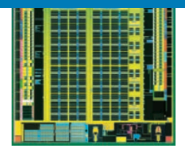

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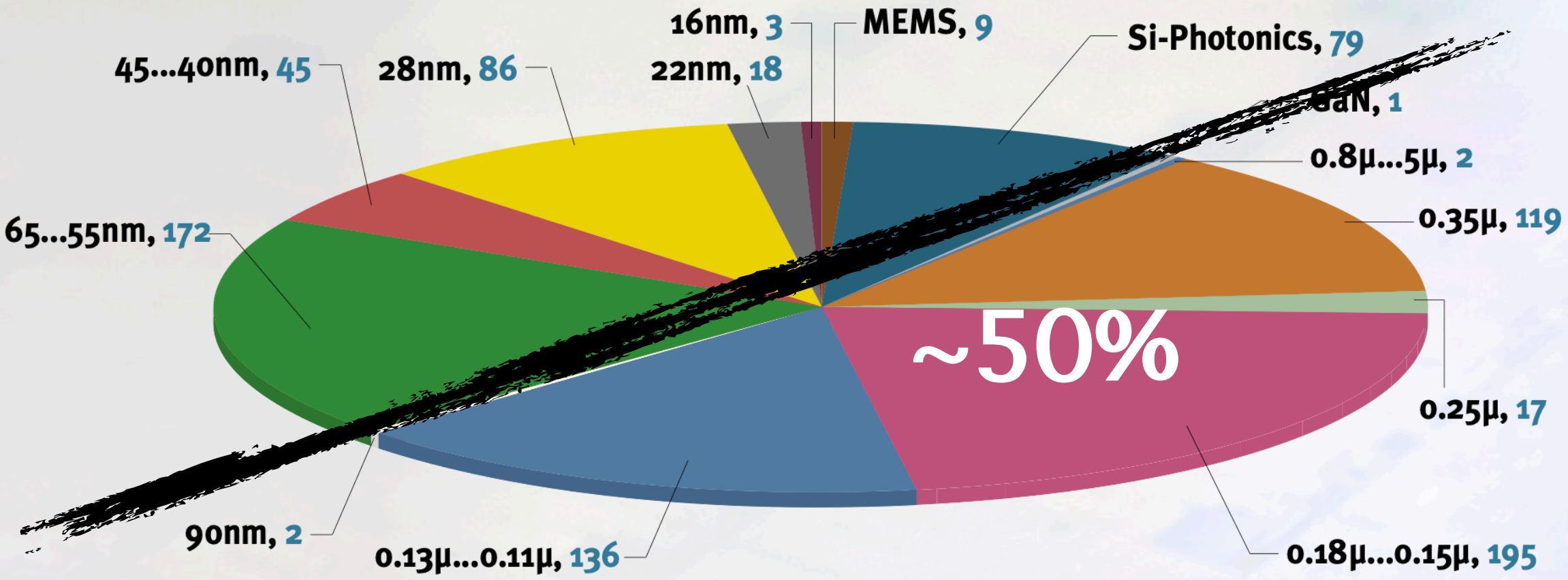
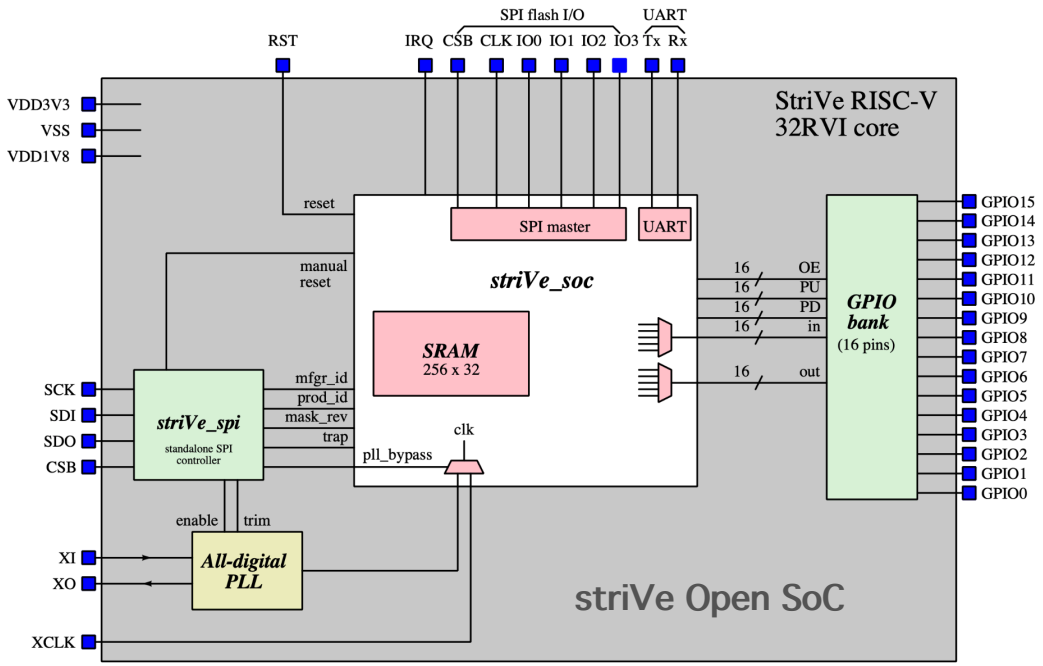


Number of fabricated designs in 2019 per technology (node)

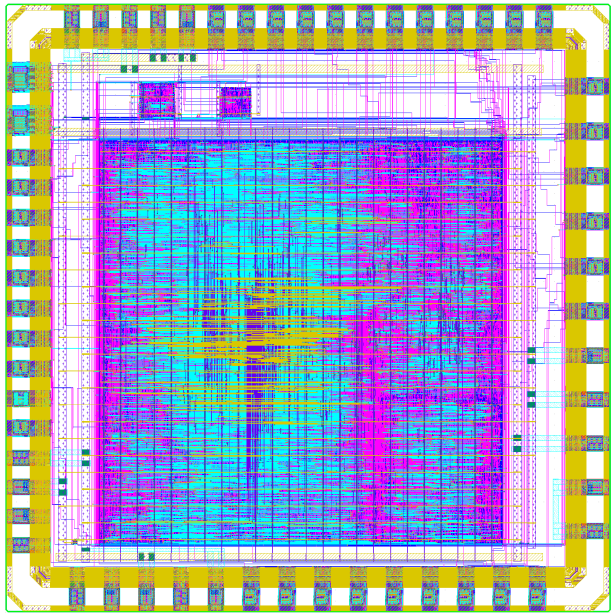
EUROPRACTICE
ASIC SERVICE

StriVe SoC Family

striVe RISC-V SoC SKY130



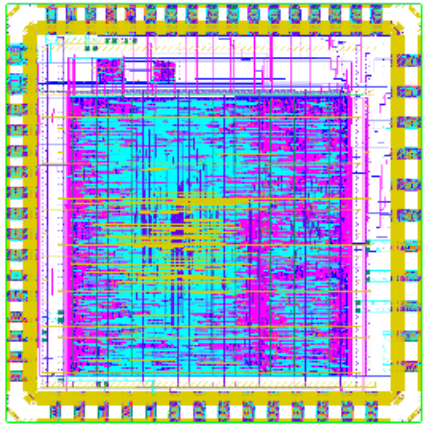
striVe SW130nm (2.743 x 2.751 mm^2)



striVe RISC-V SoC

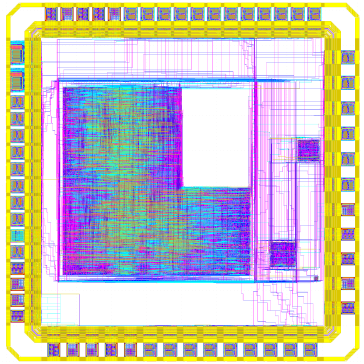
SkyWater sky130

striVe



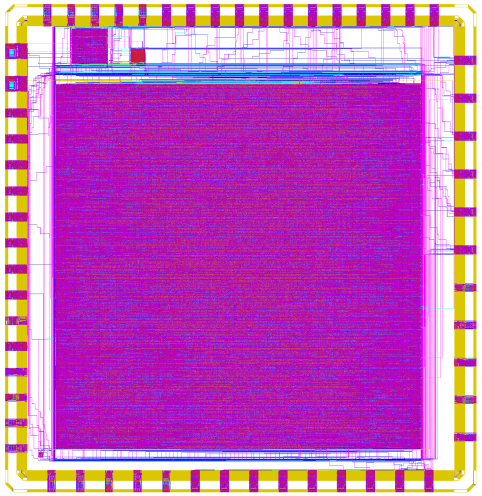
2.743 x 2.751 mm^2

striVe2



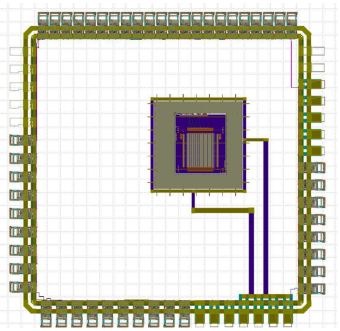
2.013 x 2.042 mm^2

striVe3



4.301 x 4.451 mm^2

openram_tc_1kb



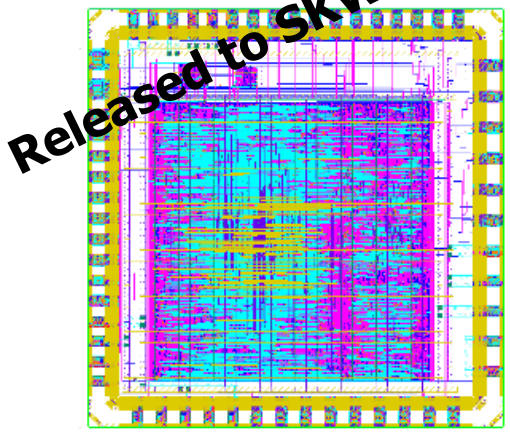
2.013 x 2.042 mm^2

skywater TECHNOLOGY FOUNDRY Google OpenROAD efabless.com

striVe RISC-V SoC

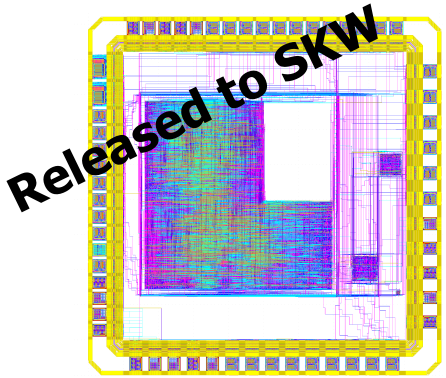
SkyWater sky130

striVe



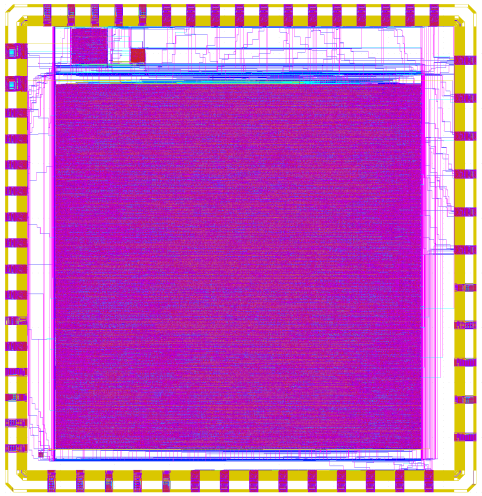
2.743 x 2.751 mm²

striVe2



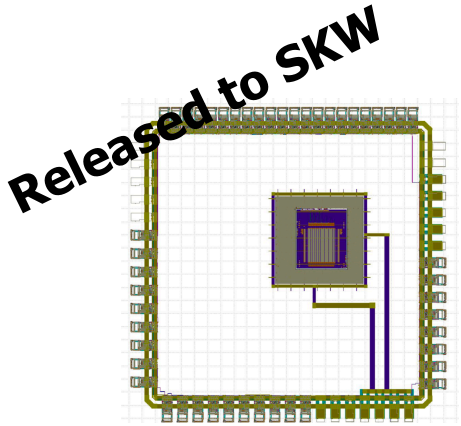
2.013 x 2.042 mm²

striVe3



4.301 x 4.451 mm²

openram_tc_1kb



2.013 x 2.042 mm²

skywater TECHNOLOGY FOUNDRY Google OpenROAD efabless.com

striVe Features Details

IC	CPU	Standard Cells	Memory Size (kbytes)	Memory Type	Extra Features
strive	PicoRV32	**fd**_sc_**hd**	1	Logic RAM (DFF)	
strive2	PicoRV32	**fd**_sc_**hd**	1	**OpenRAM**	
strive3	PicoRV32	**osu**_sc	1	Logic RAM (DFF)	
strive4	PicoRV32	**osu**_sc	1	**OpenRAM**	
strive5	PicoRV32	**fd**_sc_**hd**	**8**	**OpenRAM**	
strive6	PicoRV32	**fd**_sc_**hd**	1	**OpenRAM**	DFT

Initial Open SoC Plans

efabless.com

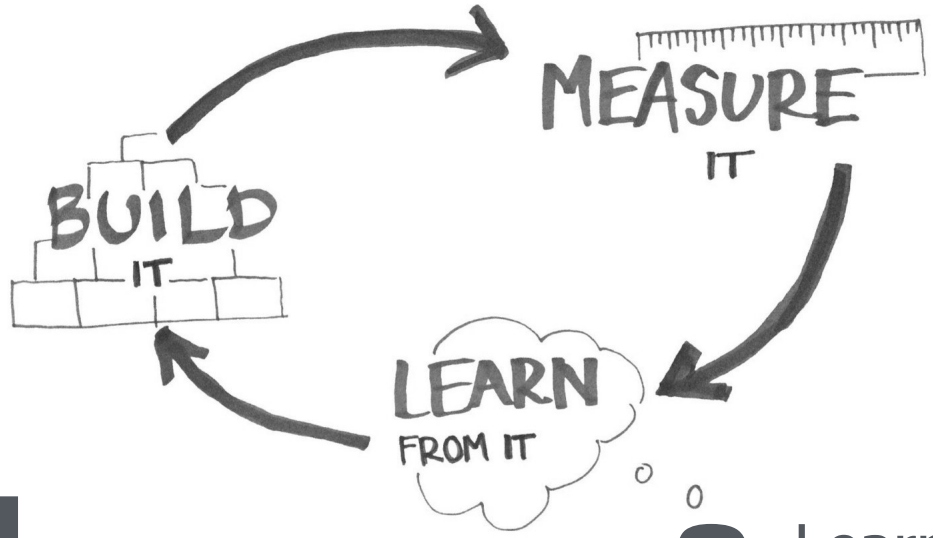
What’s Next?

BUILD-MEASURE-LEARN-REFINE

Design it
Build it **1**

Quick
Cheap

2 Give it to users to test in their use case



3 Learn from it, viability, feasibility, desirability

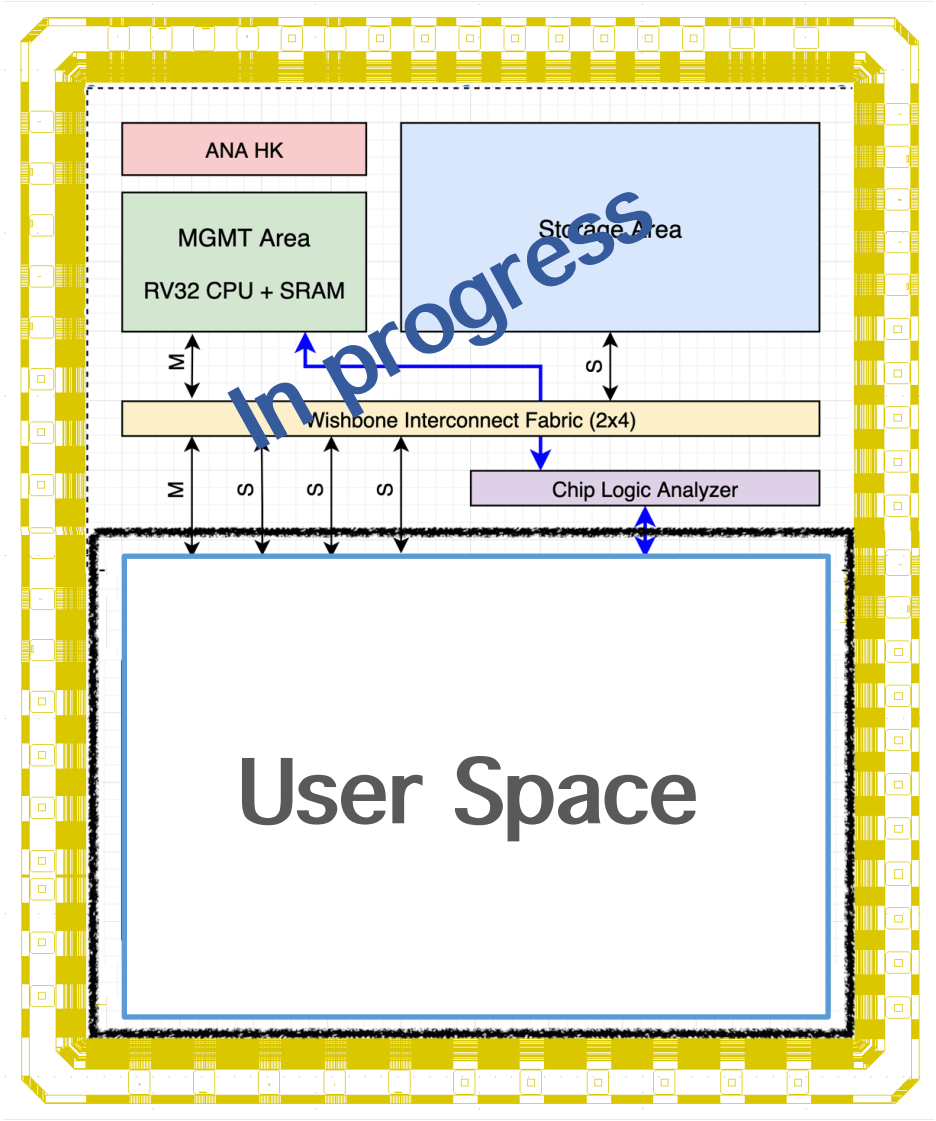
Do it Again
Many times **4**

Open source shuttle program!

Google + efabless.com

~ Nov 30, 2020

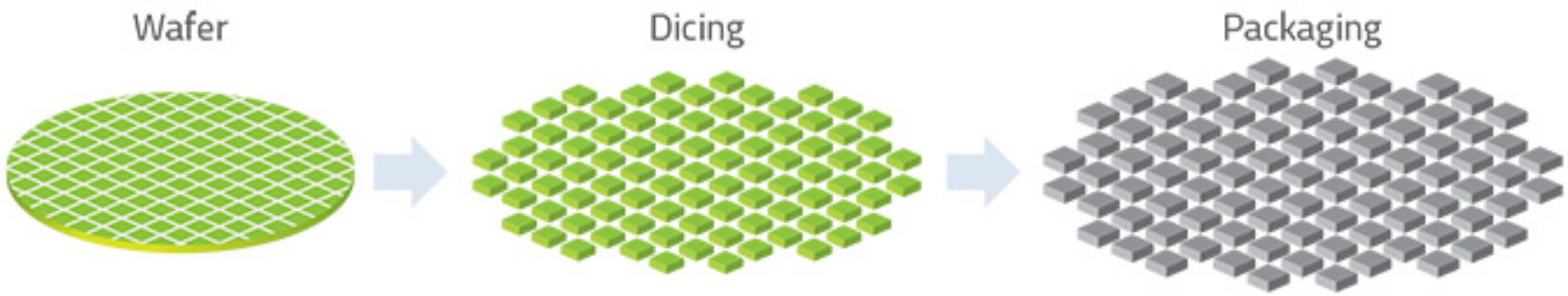
- Standard Harness Setup
- Management/User resources
- 40 open slots
- ~100parts & 5 harness boards
- Stay tuned for the spec in a couple of weeks



Caravel SoC

Caravel Packaging WCSP

STD

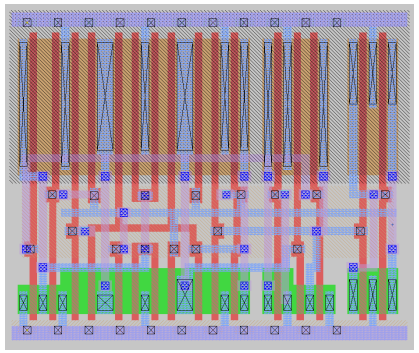


WCSP

Join the Team & Contribute

- The SkyWater PDK Slack Space - https://join.skywater.tools
- The OpenLane flow for digital PnR can be found at https://openlane.io
- The documentation is at https://docs.skywater.tools

Future Dialup Talks



Designing new cells for SkyWater 130nm

James Stine

Tuesday, September 22, 2020 16:00 GMT

OpenRAM

UC SANTA CRUZ

OpenRAM on SkyWater 130nm

Matt Guthaus

Tuesday, October 20, 2020 16:00 GMT

Magic VLSI Layout Tool

Current distribution version 8.2

Magic for DRC checks on SkyWater 130nm

Tim Edwards

Tuesday, November 17, 2020 16:00 GMT

efabless.com

One Big Team

Open Source SkyWater PDK

Google

skywater TECHNOLOGY

Open Source MPW Shuttle Program

Google

efabless.com

Industry partners

antmicro

efabless.com

BLUE CHEETAH ANALOG DESIGN

Academic partners

THE AMERICAN UNIVERSITY IN CAIRO

Ohio Supercomputer Center
An OH·TECH Consortium Member

UC SANTA CRUZ

UC San Diego

(Common Hardware for Interfaces, Processors and Systems) CHIPS

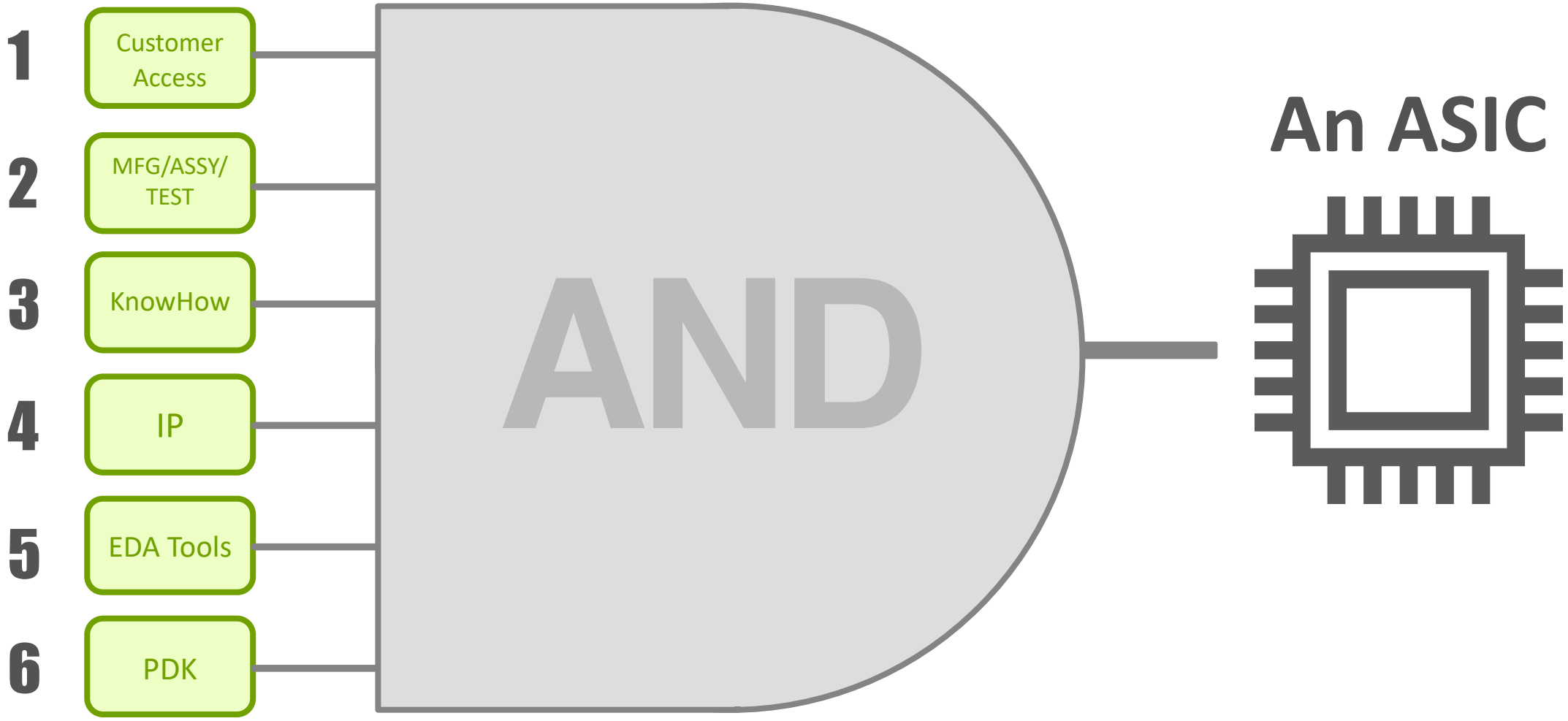
Organization that develops open source hardware RTL and open source software design tools

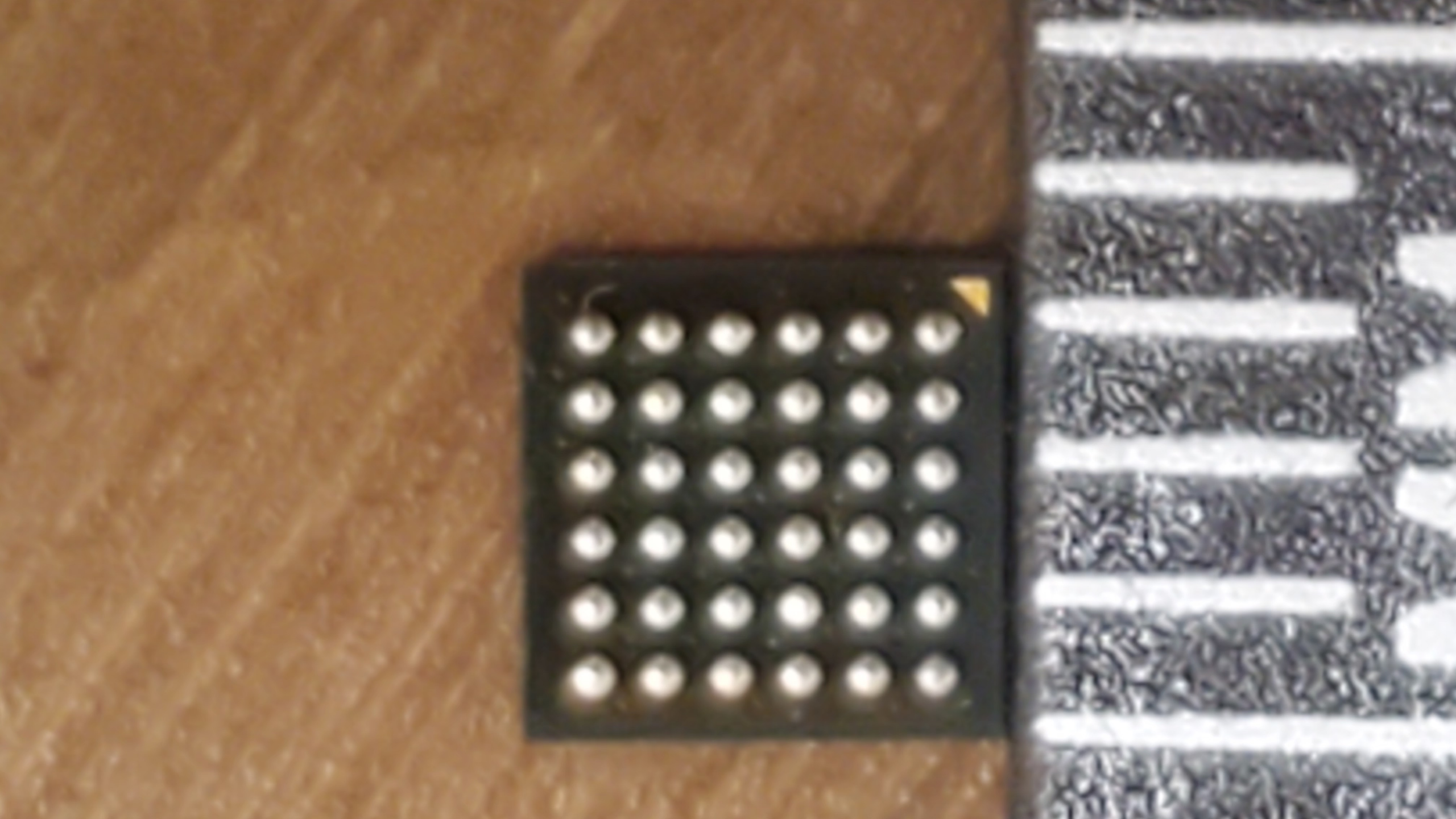
THANK YOU

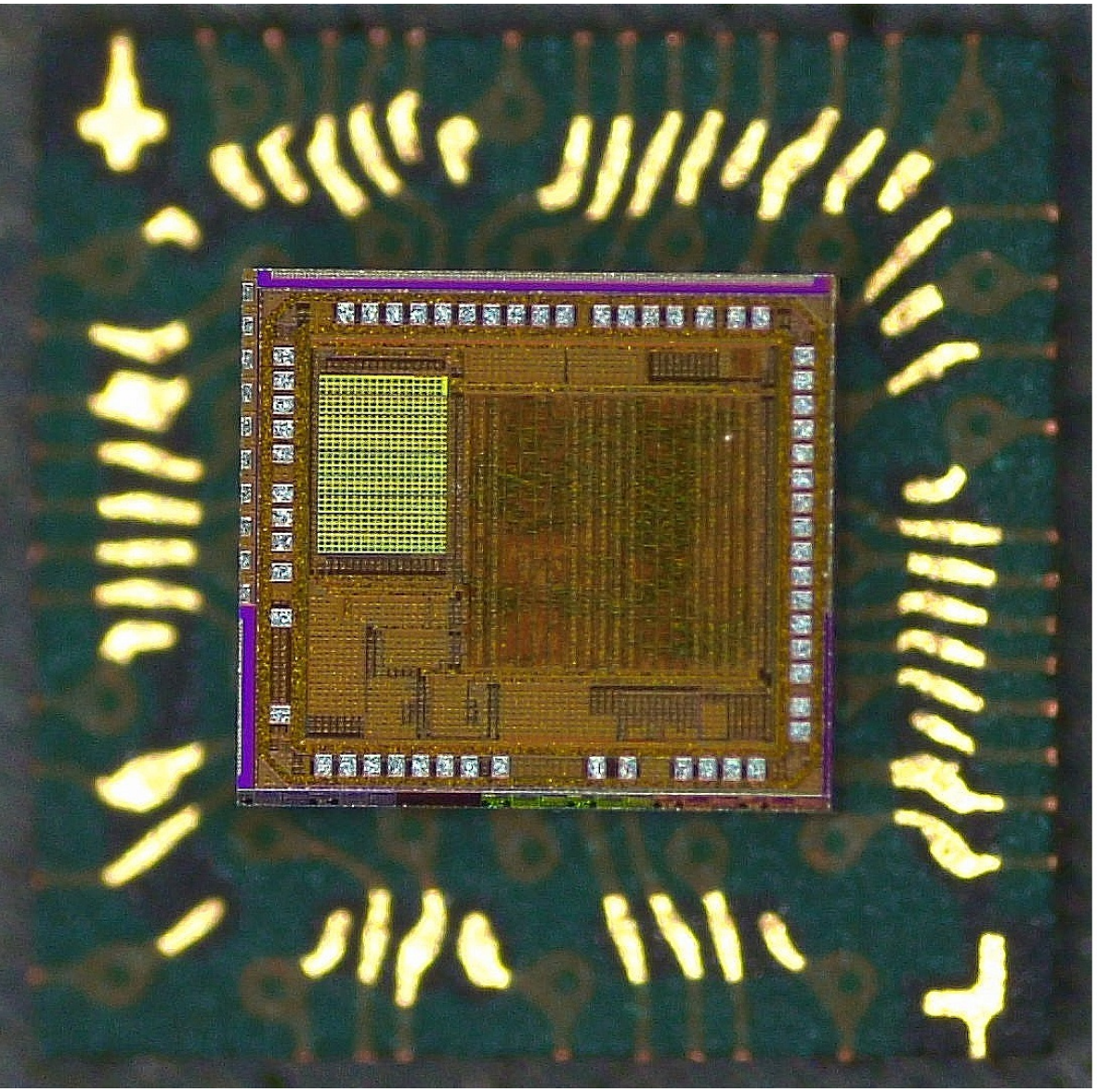
— Questions —

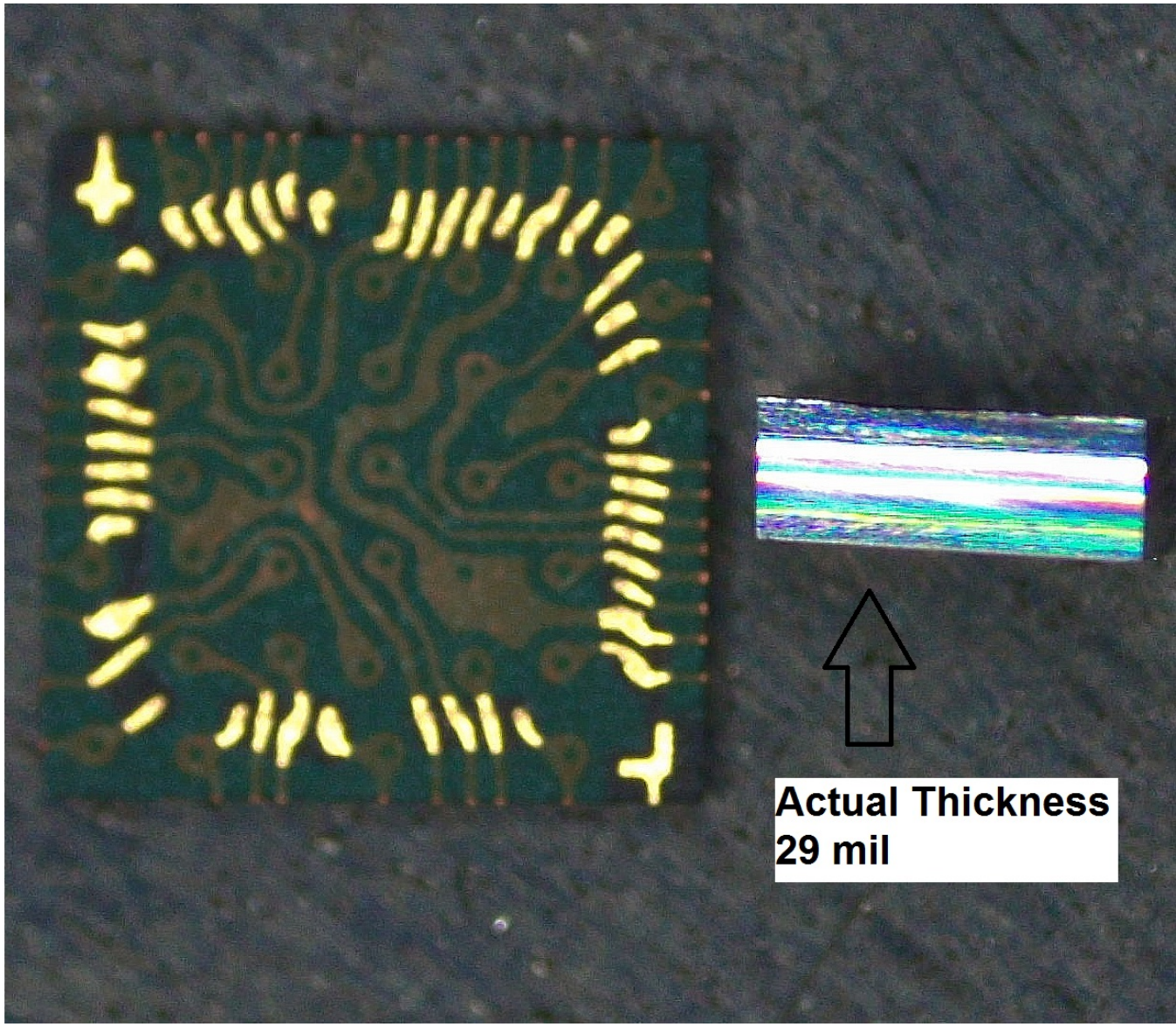
Backup Slides

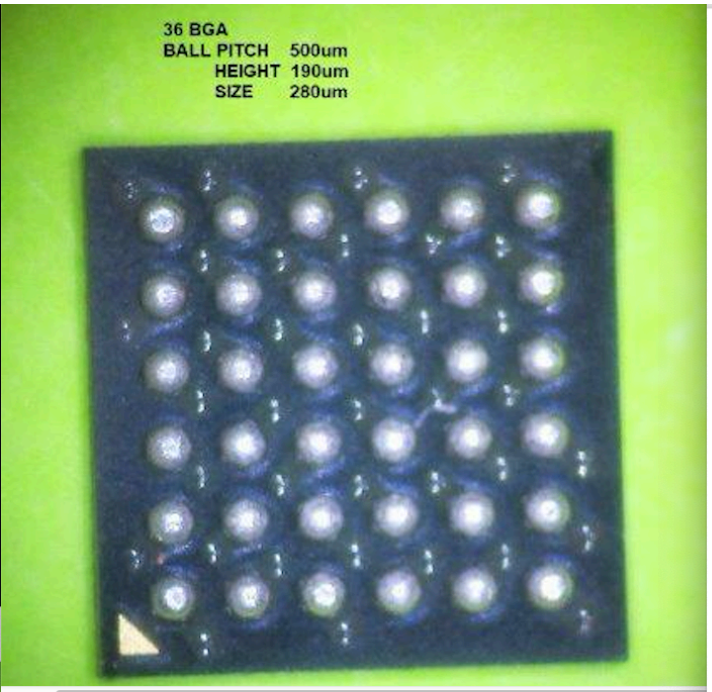
WHAT'S NEEDED TO DESIGN



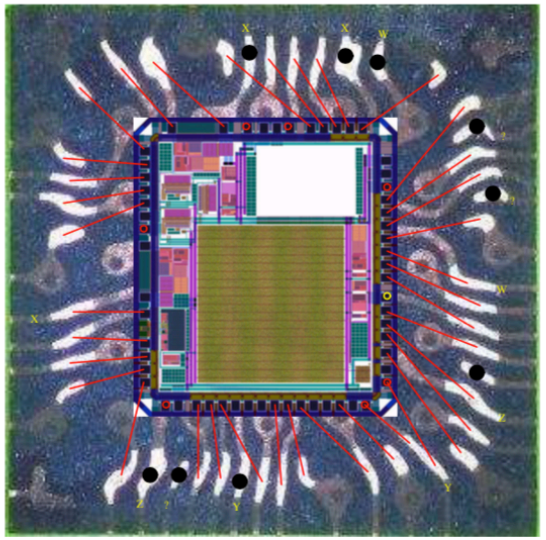


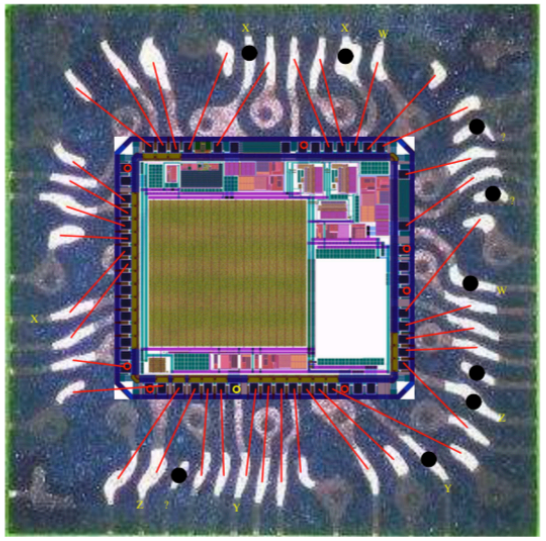


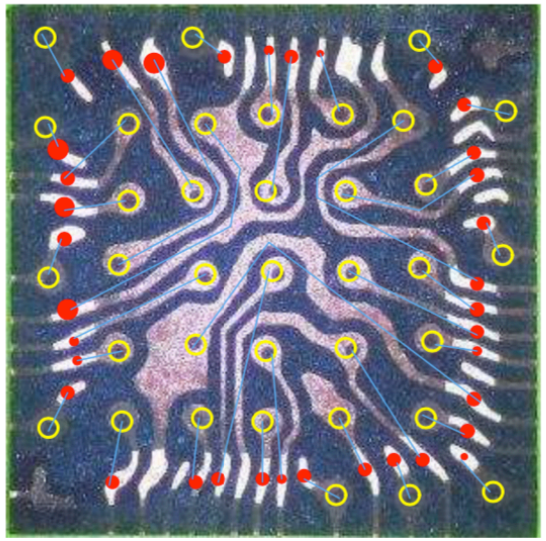

Actual Thickness
29 mil



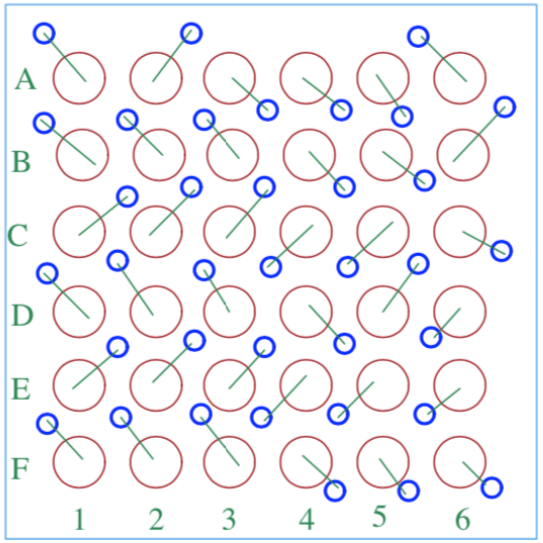
Preferred bonding

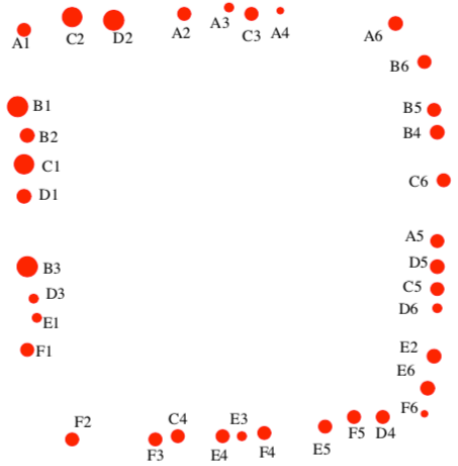






Available unique wirebond pads





Preferred bonding pinout

A1	ANALOG_OUT	D1	ADC0_IN
A2	COMP_INP	D2	VDD1V8
A3	COMP_INN	D3	XO
A4	SER_TX	D4	VSS
A5	FLASH_IO1	D5	FLASH_IO2
A6	SER_RX	D6	SDO
B1	VREF_H	E1	GPIO[0]
B2	VREF_L	E2	SCK
B3	XI	E3	GPIO[9]
B4	FLASH_CSB	E4	GPIO[5]
B5	FLASH_CLK	E5	GPIO[11]
B6	XCLK	E6	CSB
C1	ADC1_IN	F1	GPIO[1]
C2	VDD3V3	F2	GPIO[2]
C3	IRQ	F3	GPIO[3]
C4	GPIO[4]	F4	GPIO[10]
C5	FLASH_IO3	F5	GPIO[15]
C6	FLASH_IO0	F6	SDI

KLayout 0.26.4 - striVe_FILL.sto.gds [striVe]

Back | Forward | Select | Move | Ruler | Add | Polygon | Box | Text | Path | Instance | Partial | EFS8A

Cells

striVe

Levels 0 .. 3

Navigator

Options

striVe

striVe_FILL.sto.gds [striVe]

40 µm

Layers

202/0@1
cctm1.mask - 35/0 - 35/0@1
cdnm.mask - 48/0 - 48/0@1
cfom.mask - 23/0 - 23/0@1
chvntm.mask - 39/0 - 39/0@1
chvtpm.mask - 97/0 - 97/0@1
chvtrm.mask - 98/0 - 98/0@1
cldntm.mask - 11/0 - 11/0@1
cli1m.mask - 56/0 - 56/0@1
clicm1.mask - 43/0 - 43/0@1
clvom.mask - 46/0 - 46/0@1
clvtnm.mask - 25/0 - 25/0@1
cmm1.mask - 36/0 - 36/0@1
cmm2.mask - 41/0 - 41/0@1
cmm3.mask - 34/0 - 34/0@1
cmm4.mask - 51/0 - 51/0@1
cmm5.mask - 59/0 - 59/0@1
cnpc.mask - 49/0 - 49/0@1
cnsdm.mask - 30/0 - 30/0@1
cnsm.mask - 22/0 - 22/0@1
cntm.mask - 27/0 - 27/0@1
cnwm.mask - 21/0 - 21/0@1
conom.mask - 88/0 - 88/0@1
cp1m.mask - 28/0 - 28/0@1
cpbo.mask - 99/0 - 99/0@1
cpdm.mask - 37/0 - 37/0@1
cpmm2.mask - 94/0 - 94/0@1
cpsdm.mask - 32/0 - 32/0@1
crpm.mask - 96/0 - 96/0@1
ctunm.mask - 20/0 - 20/0@1
cviam.mask - 40/0 - 40/0@1
cviam2.mask - 44/0 - 44/0@1
cviam3.mask - 50/0 - 50/0@1
cviam4.mask - 58/0 - 58/0@1

Layer Toolbox

Color
Frame color
Stipple
Animation
Style
Visibility

T EFS8A G selected: box(1099720,3846125 1103800,3850205) on cfom.mask - 23/0 - 23/0@1 in striVe/ICV_153@1 xy 1098.31019 3883.73204

KLayout 0.26.4 - striVe_FILL.sto.gds [striVe]

Back | Forward | Select | Move | Ruler | Add | Polygon | Box | Text | Path | Instance | Partial | EFS8A

Cells

striVe

Levels 0 .. 3

Navigator

Options

striVe

striVe_FILL.sto.gds [striVe]

10 um

Layers

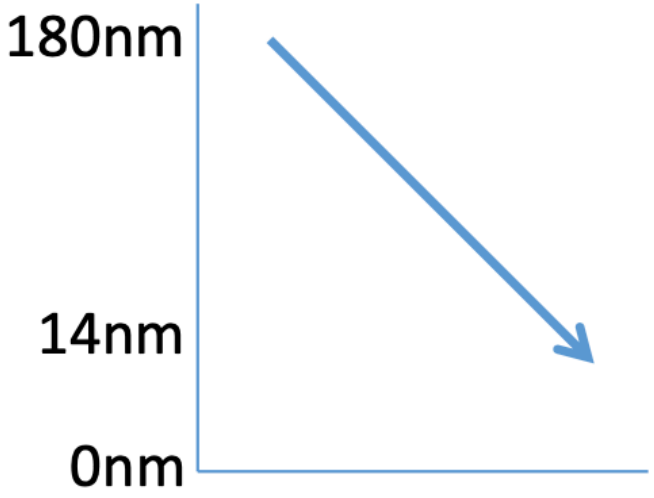
202/0@1
cctm1.mask - 35/0 - 35/0@1
cdnm.mask - 48/0 - 48/0@1
cfom.mask - 23/0 - 23/0@1
chvntm.mask - 39/0 - 39/0@1
chvtpm.mask - 97/0 - 97/0@1
chvtrm.mask - 98/0 - 98/0@1
cldntm.mask - 11/0 - 11/0@1
cli1m.mask - 56/0 - 56/0@1
clicm1.mask - 43/0 - 43/0@1
clvom.mask - 46/0 - 46/0@1
clvtnm.mask - 25/0 - 25/0@1
cmm1.mask - 36/0 - 36/0@1
cmm2.mask - 41/0 - 41/0@1
cmm3.mask - 34/0 - 34/0@1
cmm4.mask - 51/0 - 51/0@1
cmm5.mask - 59/0 - 59/0@1
cnpc.mask - 49/0 - 49/0@1
cnsdm.mask - 30/0 - 30/0@1
cnsm.mask - 22/0 - 22/0@1
cntm.mask - 27/0 - 27/0@1
cnwm.mask - 21/0 - 21/0@1
conom.mask - 88/0 - 88/0@1
cp1m.mask - 28/0 - 28/0@1
cpbo.mask - 99/0 - 99/0@1
cpdm.mask - 37/0 - 37/0@1
cpmm2.mask - 94/0 - 94/0@1
cpsdm.mask - 32/0 - 32/0@1
crpm.mask - 96/0 - 96/0@1
ctunm.mask - 20/0 - 20/0@1
cviam.mask - 40/0 - 40/0@1
cviam2.mask - 44/0 - 44/0@1
cviam3.mask - 50/0 - 50/0@1
cviam4.mask - 58/0 - 58/0@1

Layer Toolbox

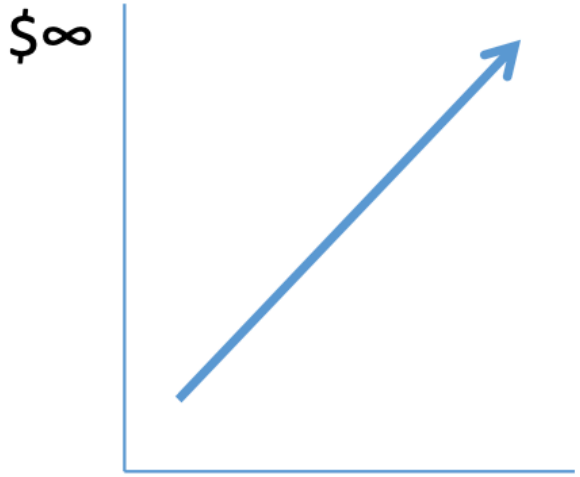
Color
Frame color
Stipple
Animation
Style
Visibility

T EFS8A G box(1981010,3336960 1981590,3337540) on cmm1.mask - 36/0 - 36/0@1 in striVe/ICV_154@1 xy 1981.48986 3337.17182

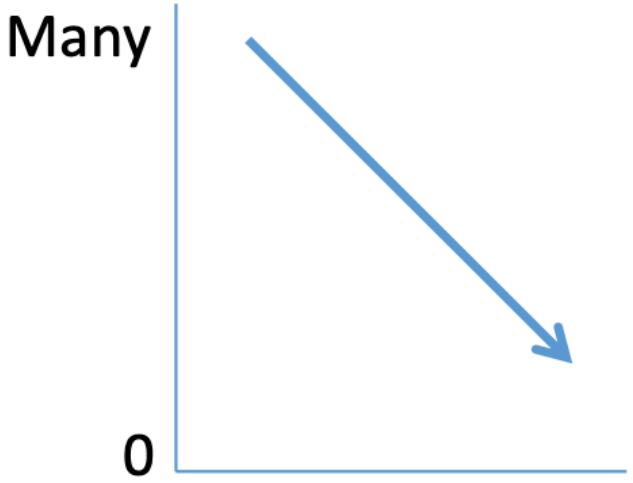
Mike’s Law ;-)



As Transistor Size Goes To Zero

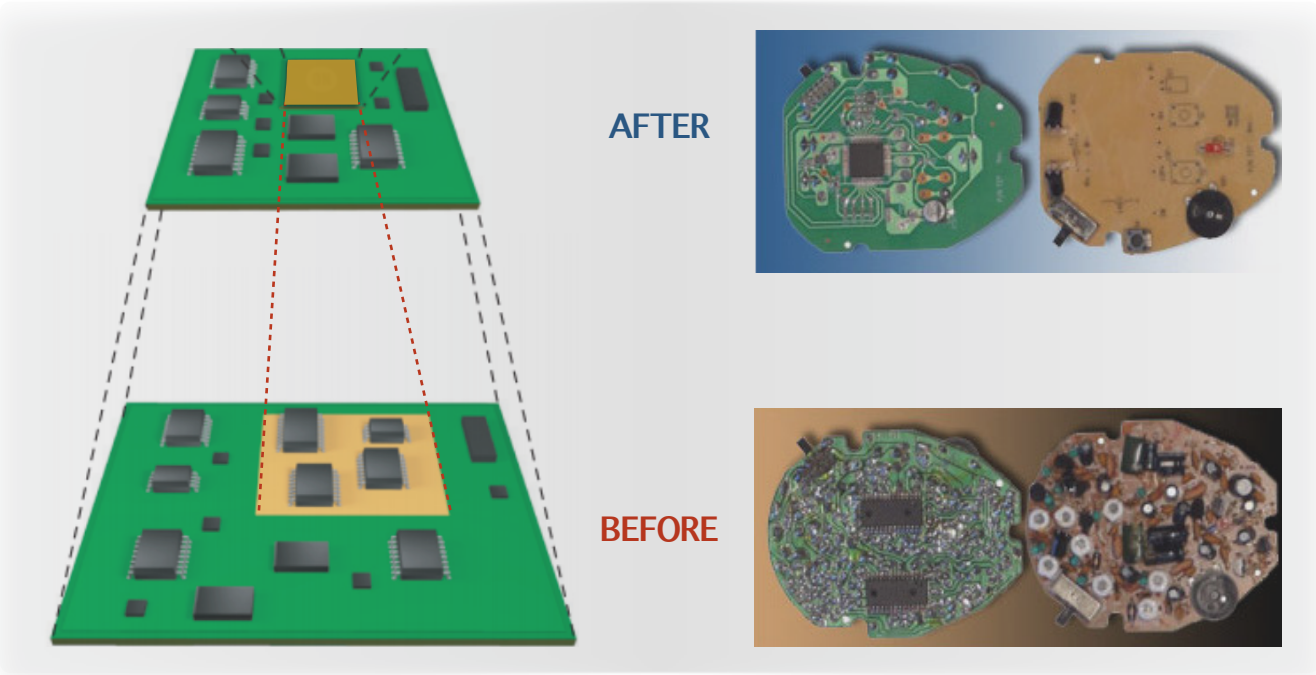


Development Cost Goes to Infinity



Number of Customers Goes to Zero

WHY CUSTOM ASICs



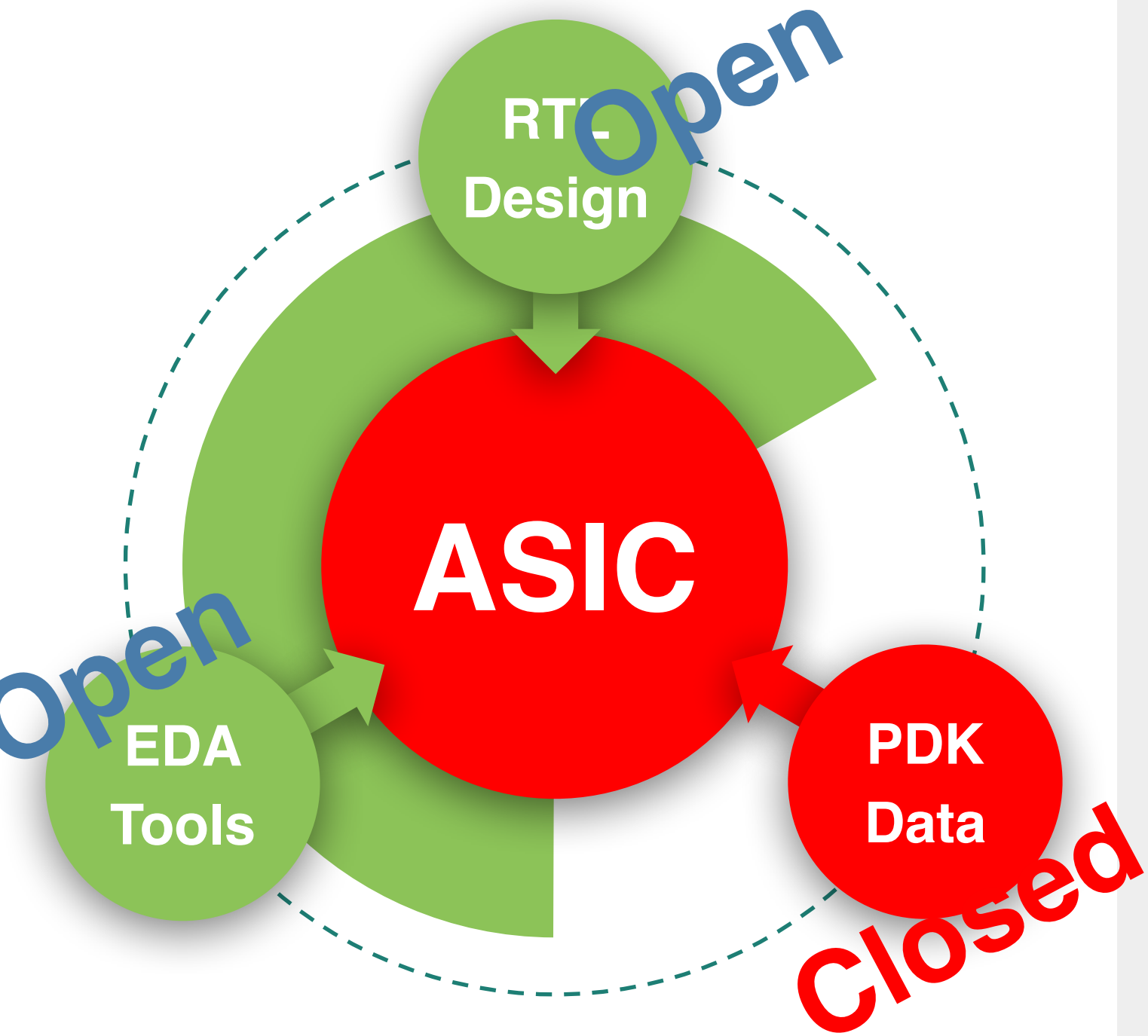
- A vast & diverse community hardware designers
- Reduce cost in your overall application
- Optimize performance and power efficiency via integration
- Reduce the size and enable superb Product Design
- Protect Intellectual Property through hardware embedding

Tim Ansell

j.mp/timtoomany-riscv

June 30, 2020

j.mp/du20-sky130



PDK Data isn't open

ASIC isn't OPEN

j.mp/du20-sky130

OpenLANE

Fully automated FOSS RTL to GDSII based on OpenROAD

Mohamed Shalan

Tuesday, July 28, 2020
16:00 GMT

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Manar A.Elatty